Future implementations of adaptive and proactive regulators

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Abstract: We will present several ideas of implementing process regulators in top fields like aeronautics, military techniques or top electronic devices which are mass produced. This vision represents what could be in the future of complex and sophisticated electronics product. Key words: future, electronic

DSP IMPLEMENTATION

DSP (**D**igital **S**ignal **P**rocessing) was especially designed for real time processing and it is based on Harvard architecture, meaning that the data and program memories are separate entities. It has special instructions for big amount of data, the so called **SIMD** instructions (**S**ingle **I**nstruction **M**ultiple **D**ata); also a general characteristic of all DSPs is the large amount of bits per word: 16, 32, 64 (there are DSP with 256 bits/word). DSP process digital signal acquired from an **A/D** (**A**nalog / **D**igital) converter and the processing result is delivered to another converter type D/A (**D**igital / **A**nalog) (see figure below).

Figure 1. DSP Structure and functioning

Certain DSPs contain, from the hardware point of view, A/D and D/A converters, as an example Z86C95 (8) . Their development is rapid due to the fact that applications with great amount of volume like fast communication, sophisticated weapons, have pushed higher the characteristics of such a device.

Signal processing can be done in any general use microprocessor, but the DSPs are especially structured for the purpose of high speed processing. Mainly it is about:

1. Harvard architecture
2. Having a memory architecture which allows fetching multiple data/instructions in the same time;
3. **DMA** (**D**irect **M**emory **A**ccess)
4. big length of the data word on which it work
5. the execution in a single cycle of any instruction, and;
6. a set of instruction adequate to mathematical processing (multiplication and division in mobile coma in a cycle on 16, 32 or 64 bits)

This addition compared to microprocessor lead to lower costs, reduced power, reduced heating of the DSP.

FPGA IMPLEMENTATION

Another modern solution which will gain more field in the cases of complex algorithms which has to be resolved in real time and adaptive regulators implementation is the insertion of all of these using logical area, **FPGA** (**F**ield **P**rogrammable **G**ate **A**rray). FPGA devices were introduced to all critical application in which time resource is limited. Subsequently, in all the cases in which

are required powerful algorithm and, eventually, led on large data words (32, 64 or more). Powerful algorithm can be gathered and solved in one or more machine clocks, these creating an important advantage from the algorithm which is implemented using a process computer by program sequences. This will be the new line of development of all critical control applications from top fields: aviation, rockets, industrial atomic stations, etc. There are so fast that can emulate general known microprocessors. In our country, at Brasov it was developed this technology, crating design firms in FPGA, which develop cabled logic for important companies in California, USA and Japan.

Between the known advantages of such devices is large density, or otherwise seen: small space, lower consumption of power. In certain projects and configuration it can reach to consumption, in standby mode, very low under 10µA, almost 0.

Another advantage of this "design tools" is the small amount of time which is done in the designing and testing phase, which in actual terms of competition and speed development represents an essential advantage. In the same time with the density and speed growth, and in general of the operational capabilities, FPGAs have taken over more complex functions, becoming system on chip (SOC).

Current FPGA applications include medical imagistic, artificial vision, voice recognition, cryptography, hardware emulation and computer firmware, aero-spatial and military applications.
In technical literature regarding the adaptive control there hadn't appear mentions about different physical implementations, but the idea will appear, if it didn't already, in the military field.

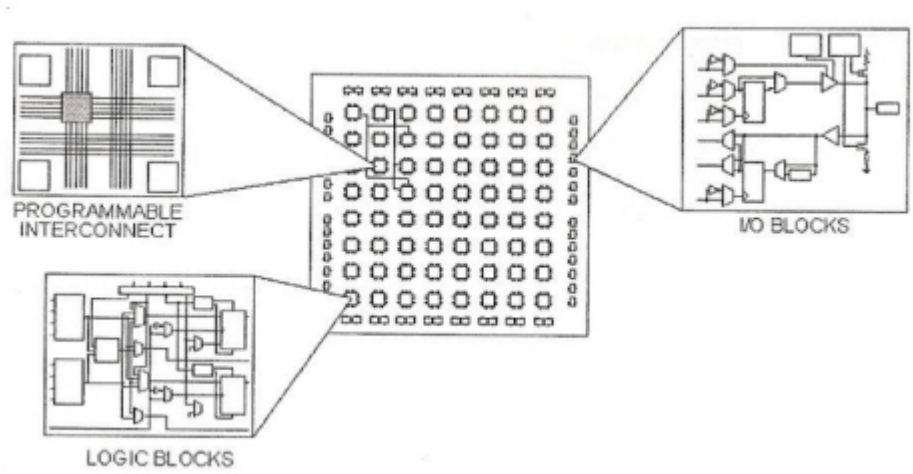

Figure 2 Internal structure FPGA

Structural paralelism of the logic resources allow FPGA to reach computetional power up to 500 MHZ. 2007 FPGA generations can implement around 100 float coma operations at each machine cycle.These capabilities have led to the developement of a new concept – reconfigurable computing.

It is remarcable that some FPGA circuits, available today, can integrate even complex processor architectures like ARM (RISC processor

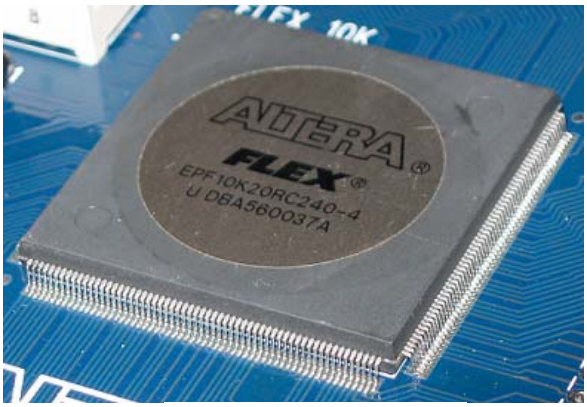

Figure 3. FPGA

on 32 bits) developed by ACORN Computers or POWERPC from APPLE, etc.

In general the designers of these architectures avoid to public their details, for obvious reasons. On the other hand, “open source” projects have begun to be popular using FPGAs.

ASIC IMPLEMENTATION

An **ASIC (A**pplication **S**pecific **I**ntegrated **C**ircuit) is a special integrated circuit produced for a certain technical application, in other words “specialized”. In general, this type of circuits groups a large number of unique functions, created accordingly to exact requirements of the application.

A typical example of ASIC in civil field is that of the mobile phone; in military field are chips from a rocket or satellite which process images in real time, or in the field of consumption in digital photographic devices which manage the entire device. The advantages of the integration of multiple functions in a single circuit are fabrication cost reduction (for mass production) and reliability enhancement. ASIC inconveniences are the development costs and design which can be expensive (especially for engraving masks) and also the development life cycle which takes several months. A new electronic device of ASIC type is programmed in a “hardware description language” VHDL, Verilog, etc. Are used same description languages for prototype and pre-series realization of logical programming ASIC circuits or FPGA.

Due to initial high costs, the production of ASIC is recommended for large volumes (several thousand hundreds units/year), to which production costs are redeemable and is not sensible to TTM (**T**ime **T**o **M**arket) or on other words do not age till they are lunched on the market. An exception is represented when the client, from strategic interests, risks and pays, the desired functionality, even though the fabrication volume is small.

Some complex ASICs are named **SoC** (**S**ystem **O**n **C**hip), and this tpe of ASIC represent “system on a single silicon pill”. SoC can be integrated in a microprocessors central unit (or even more), interfaces, memories, etc., incorporating a number of several million of logic gates and ensuring a level of functionality equal, for example, with that of a computer motherboard.

The disadvantage of a solution different than ASIC consists of the fact that for a given logic function, its realization in FPGA offers modest performances (from the speed point of view) in comparison with ASIC. On the other hand, considering that the production costs and especially design of an ASIC, often prohibited, it is often imposed the usage of FPGA for different applications.